



2183

PTO/SB/21 (09-04)

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/838,678	
	Filing Date	April 19, 2001	
	First Named Inventor	Uht, Augustus K.	
	Art Unit	2183	
	Examiner Name	O'BRIEN, BARRY J.	
Total Number of Pages in This Submission	12	Attorney Docket Number	022193-010310US

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Date	March 21, 2005	Reg. No.	37,478

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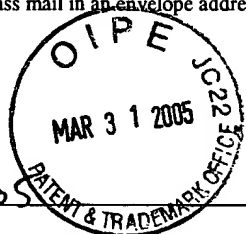
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PATENT
Attorney Docket No.: 022193-010310US
Client Reference No.: URI-165

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Augustus K. Uht et al.

Application No.: 09/838,678

Filed: April 19, 2001

For: AUTOMATIC AND
TRANSPARENT HARDWARE
CONVERSION OF TRADITIONAL
CONTROL FLOW TO PREDICATES

Examiner: O'BRIEN, BARRY J.

Art Unit: 2183

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT UNDER 37
CFR §1.97 and §1.98

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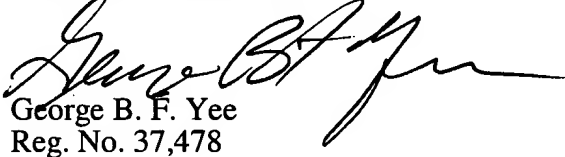
The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no

representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,


George B. F. Yee
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	Agerwala et al., "Data Flow Systems - Special Issue," <i>IEEE COMPUTER</i> , vol. 15, no. 2, pp. 10-13, 1982.	
	2	Aiken et al., "Perfect Pipelining: A New Loop Parallelization Technique," in <i>Proceedings of the 1988 European Symposium on Programming</i> , 1988, 15 pages total.	
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	4	Banerjee et al., "Fast Execution of Loops With IF Statements," <i>IEEE Transactions on Computers</i> , vol. C-33, pp. 1030-1033, November 1984.	
	5	Beck et al., "The cydra 5 minisupercomputer: Architecture and implementation," <i>Journal of Supercomputing</i> , vol. 7, pp. 143-180, 1993.	
	6	Brekelbaum et al., "Hierarchical Scheduling Windows," in <i>Proceedings of the 35th Annual International Symposium on Microarchitecture</i> . Istanbul, Turkey: IEEE, ACM, November 2002.	
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	15	Cragon, <i>Branch Strategy Taxonomy and Performance Models</i> , Los Alamitos, California: IEEE Computer Society Press, 1992, 9 pages total.	
	16	Cytron, "Doacross: Beyond Vectorization for Multiprocessors (Extended Abstract)," in <i>Proceedings of the 1986 International Conference on Parallel Processing</i> , pp. 836-844, Pennsylvania State University and the IEEE Computer Society, August 1986.	
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	17	Dutta et al., "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors," in <i>Proceedings of the 28th International Symposium on Microarchitecture (MICRO-28)</i> , pp. 258-263, IEEE and ACM, November/December 1995.	
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	32	Henry et al., "The Ultrascalar Processor: An Asymptotically Scalable Superscalar Microarchitecture," in <i>HIPC '98</i> , December 1998, URL: http://ee.yale.edu/papers/HIPC98-abstract.ps.gz , 18 pages total.	

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	33	Huck et al., "Introducing the ia-64 architecture," in <i>IEEE Micro</i> , pp. 12-23, September 2000.	
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	38	Kim et al., "An Instruction Set Architecture and Microarchitecture for Instruction Level Distributed Processing," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> . Anchorage, Alaska, USA: ACM, May 25-29, 2002.	
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	43	Lam et al., "Limits of Control Flow on Parallelism," in <i>Proceedings of the 19th Annual International Symposium on Computer Architecture</i> . Gold Coast, Australia: IEEE and ACM, May 1992, pp. 46-57.	
	44	Lebeck et al., "A Large, Fast Instruction Window for Tolerating Cache Misses," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> . Anchorage, Alaska, USA: ACM, May 25-29, 2002, 12 pages total.	
	45	Lee et al., "Branch Prediction Strategies and Branch Target Buffer Design," <i>COMPUTER</i> , vol. 17, pp. 6-22, January 1984.	
	46	Lepak et al., "On the value locality of store instructions," in <i>Proceedings of the International Symposium on Computer Architecture</i> , pp. 182-191, June 2000.	
	47	Lilja, "Reducing the Branch Penalty in Pipelined Processors," <i>COMPUTER</i> , vol. 21, pp. 47-55, July 1988.	

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	48	Lipasti et al., "Superspeculative Microarchitecture for Beyond AD 2000," <i>IEEE COMPUTER</i> , vol. 30, no. 9, pp. 59-66, September 1997.	
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	52	Morano et al., "Implications of Register and Memory Temporal Locality for Distributed Microarchitectures," Dept. of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA, Technical Report, October 2002, pp 1-20, URL: http://www.ece.neu.edu/groups/nucar/publications/interval_ls.pdf	
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	56	Pajuelo et al., "Speculative Dynamic Vectorization," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> , Anchorage, Alaska, USA: ACM, May 25-29, 2002.	
	57	Papworth, "Tuning the Pentium Pro Microarchitecture," <i>IEEE MICRO</i> , vol. 16, no. 2, pp. 8-15, April 1996.	
	58	Parcerisa et al., "Efficient Interconnects for Clustered Microarchitectures," in <i>Proceedings of the Eleventh International Conference on Parallel Architectures and Compilation Techniques</i> , Charlottesville, Virginia, USA: IEEE, September 22-25, 2002 10 pages total.	
	59	Park et al., "Reducing Register Ports for Higher Speed and Lower Energy," in <i>Proceedings of the 35th Annual International Symposium on Microarchitecture</i> , Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
	60	Patt et al., "HPS, a New Microarchitecture: Rationale and Introduction," in <i>Proceedings of the Eighteenth Annual Workshop on Microprogramming (MICRO-18)</i> : IEEE and ACM, December 1985, pp. 103-108.	
	61	Popescu et al., "The Metaflow Architecture," <i>IEEE MICRO</i> , vol. 11, no. 3, June 1991, pp. 10-13 & 63-73.	

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	62	Preston et al., "Design of an 8-wide Superscalar RISC Microprocessor with Simultaneous Multithreading," in <i>Proceedings of the International Solid State Circuits Conference</i> , January 2002. Slides from talk at conference also referenced, 6 pages total.	
	63	Raasch et al., "A Scalable Instruction Queue Using Dependence Chains," in <i>Proceedings of the 29th Annual International Symposium on Computer Architecture</i> . Anchorage, Alaska, USA: ACM, May 25-29, 2002, 12 pages total.	
	64	Rau et al., "Instruction-level parallel processing: History, overview and perspective," <i>International Journal of Supercomputing</i> , vol. 7, pp. 9-50, October 1996.	
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	70	Sazeides et al., "The Performance Potential of Data Dependence Speculation & Collapsing," in <i>Proceedings of the 29th International Symposium on Microarchitecture (MICRO-29)</i> : IEEE and ACM, December 1996, pp. 238-247.	
	71	Sazeides et al., "The predictability of data values," in <i>Proceedings of the 30th International Symposium on Microarchitecture</i> , pp. 248-258, December 1997, 11 pages total.	
	72	Seznec et al., "Register Write Specialization Register Read Specialization: A Path to Complexity-Effective Wide-Issue Superscalar Processors," in <i>Proceedings of the 35th Annual International Symposium on Microarchitecture</i> . Istanbul, Turkey: IEEE, ACM, November 2002, 12 pages total.	
	73	Smith et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," in <i>Proceedings of the 17th Annual International Symposium on Computer Architecture</i> , pp. 344-354, IEEE and ACM, May 1990.	
	74	Smith, "A Study of Branch Prediction Strategies," in <i>Proceedings of the 8th Annual Symposium on Computer Architecture</i> , pp. 135-148, IEEE and ACM, 1981.	
	75	Smith, "Architecture and Applications of the HEP Multiprocessor Computer," <i>Society of Photo-optical Instrumentation Engineers</i> , no. 298, pp. 241-248, 1981.	
	76	Sohi et al., "Multiscalar processors," in <i>Proceedings of the International Symposium on Computer Architecture</i> , IEEE and ACM, pp. 414-425, June 1995.	
	77	Su et al., "GURPR - A Method for Global Software Pipelining," in <i>Proceedings of the Twentieth Annual Workshop on Microprogramming (MICRO-20)</i> , Association of Computing Machinery, pp. 88-96, December 1987.	

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Examiner Signature	Date Considered
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known		
			Application Number	09/838,678	
			Filing Date	April 19, 2001	
			First Named Inventor	Uht, Augustus K.	
			Art Unit	2183	
			Examiner Name	O'BRIEN, BARRY J.	
Sheet	8	of	8	Attorney Docket Number	022193-010310US

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	93	Wallace et al., "Threaded Multiple Path Execution," in <i>25th Annual International Symposium on Computer Architecture</i> : ACM, June 1998, pp. 238-249.	
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	97	Zahir et al., "Os and compiler considerations in the design of the ia-64 architecture," in <i>Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems</i> , pp. 212-221, November 2000.	

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